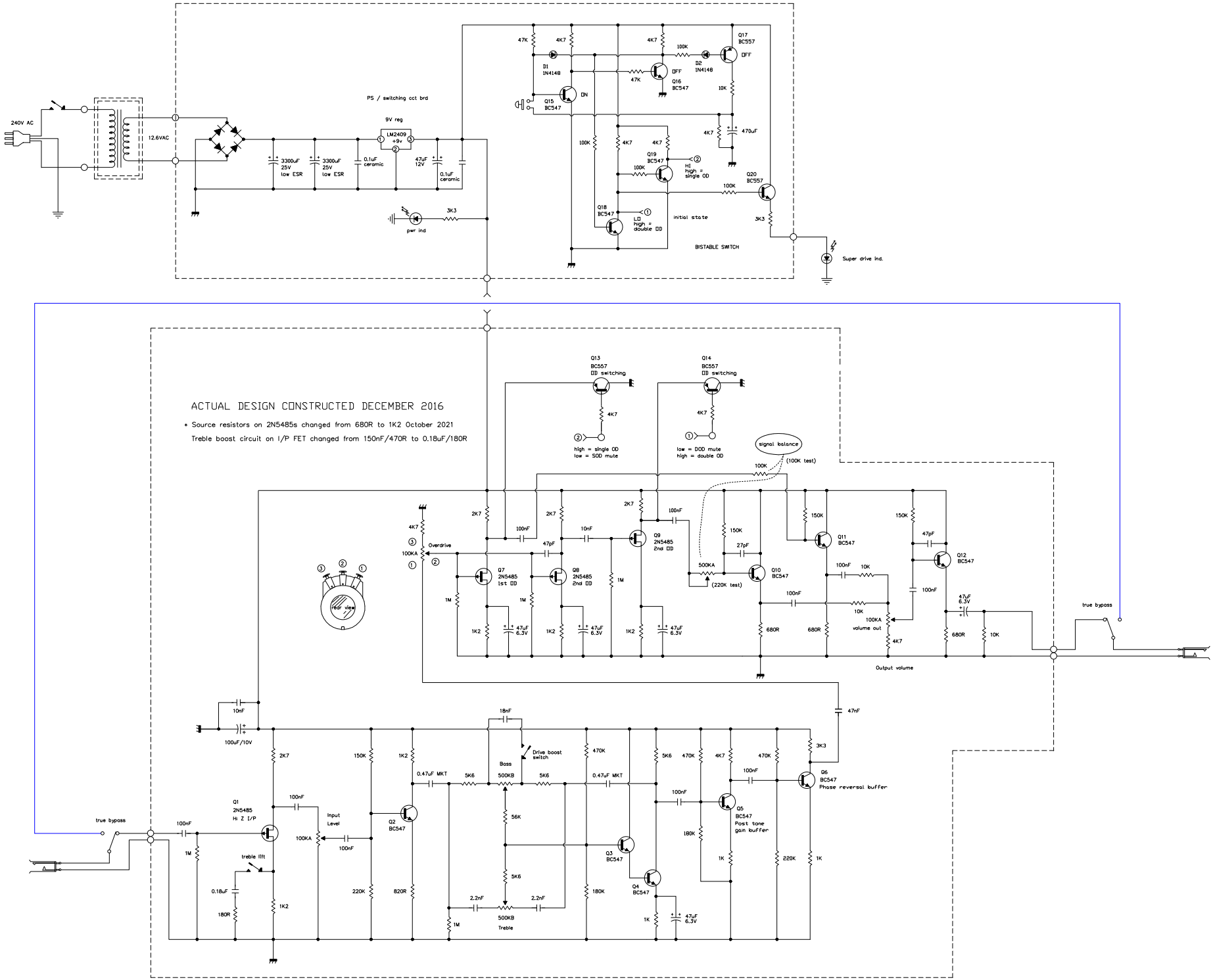
240V AC
12.6VAC
PS / switching cct brd
9V reg
LM2409
+9v
3300uF
25V
low ESR
3300uF
25V
low ESR
0.1uF
ceramic
47uF
12V
0.1uF
ceramic
3K3
pwr ind
47K
4K7
D1
1N4148
Q15
BC547
ON
4K7
Q16
BC547
OFF
100K
D2
1N4148
Q17
BC557
OFF
10K
4K7
470uF
100K
4K7
4K7
Q19
BC547
100K
HI
high =
single OD
Q20
BC557
100K
Q18
BC547
LO
high =
double OD
initial state
3K3
BISTABLE SWITCH
Super drive ind.
ACTUAL DESIGN CONSTRUCTED DECEMBER 2016
* Source resistors on 2N5485s changed from 680R to 1K2 October 2021
Treble boost circuit on I/P FET changed from 150nF/470R to 0.18uF/180R
Q13
BC557
OD switching
Q14
BC557
OD switching
4K7
high = single OD
low = SOD mute
4K7
low = DOD mute
high = double OD
signal balance
(100K test)
100K
2K7
100nF
2K7
10nF
2K7
100nF
150K
150K
150K
47pF
4K7
Overdrive
100KA
47pF
Q9
2N5485
2nd OD
27pF
Q11
BC547
Q12
BC547
Q7
2N5485
1st OD
Q8
2N5485
2nd OD
1M
1M
1M
500KA
(220K test)
Q10
BC547
100nF
10K
100nF
rear view
100nF
10K
47uF
6.3V
1K2
47uF
6.3V
1K2
47uF
6.3V
680R
680R
100KA
volume out
4K7
680R
10K
true bypass
Output volume
10nF
100uF/10V
18nF
47nF
2K7
150K
1K2
Drive boost
switch
470K
5K6
470K
4K7
470K
3K3
0.47uF MKT
5K6
Bass
500KB
5K6
0.47uF MKT
100nF
Q6
BC547
Phase reversal buffer
100nF
Q1
2N5485
Hi Z I/P
Input
Level
56K
Q5
BC547
Post tone
gain buffer
true bypass
100nF
Q2
BC547
100KA
100nF
Q3
BC547
180K
1K
220K
1K
1M
treble lift
5K6
Q4
BC547
0.18uF
180R
220K
820R
1K2
2.2nF
2.2nF
180K
1K
47uF
6.3V
1M
500KB
Treble